Silicon pad multiplicity detector for WA98

May 9, 1997

VA-1 chip was used for the front-end electronics of WA98 Silicon Pad Multiplicity Detector (SPMD). The chip contains 128 charge preamplifiers with the gain of 12.5 mV/fC, each followed by CR-RC shaper, sample and hold and analog multiplexer with differential output buffer. A **shaping time of 0.6 μs** was set in order to decrease impulse pile-up at high particle rate. The chip has a circuitry which permits to make calibration of each channel using common capacitor in *Test* mode.

Block diagram of the readout system is sketched in Fig. 1. It consists from "front-end system" interfaced with the VA1 preamplifiers, a "remote system" interfaced with the data acquisition modules, and the optical link. In order to exclude ground related problems we used optical decoupling for control signals, 4 twisted pairs for analog differential output signals and a floating power supply system.

During read-out signals go from detectors on the ceramic substrate (hybrid) through the twisted pare cables (1 m) to an intermediate amplifier buffer on Hybrid Adapter Boards (HAB) and then through a 50 m long twisted pare cable to the FADC modules in the control room.

Each quadrant of detector is equipped with its own read-out front-end electronics. There are 8 chips on each hybrid per a quadrant. The chips are glued onto hybrid circuits and the preamplifier inputs are connected to detector pads by short bonded wires. The outputs of chips on a hybrid are multiplexed, their read-out is going in sequence, according to daisy chain connection.

The *Sequencer* provides all control signals for VA1 readout and synchro-signals for "remote" FADC system. The internal logic of the data acquisition system is controlled by "state machine" with Erasable PROM, and can be easy changed.

HAB provides, also, necessary power supplies, control bias voltages and currents for VA1 chips, and works like a buffer of digital control signals from *Sequencer*. It contains a "switch" for calibration of VA1 chips in the *Test* mode. The DAC available on *Sequencer* board provides the required voltage for calibration.

The optical link consist from usual optical decoupler of the *Trigger* signal and two digital Fiber Optical Links (FOL). Because internal clock' period time of FOL (100 ns) is comparable to the peaking time of shaper (T_{hold}=0.6μs) we built separate asynchronous optically decoupled line for *Trigger* signal.

Digital FOL is built on the base of multimode fiber and *TAXI*-chips and can send only digital codes. One FOL is used for control of *Sequencer* and the second one transmits synchro-signals for FADC (VME based system of STR751/STR755). Initialization signals for *Sequencer* and digital code for DAC are sent from VME based output register AVME 9412.

There are **two modes of VA1 read-out**: one (*Normal* **mode**) during normal data taking from the detector, and the second one (*Test* **mode**) for calibration reason. In both modes the read-out of 4 quadrants is going in parallel.

In the **first mode** *Sequencer* **initialized by** *Trigger* **signal** from external logic. The *Hold* signal for VA1 chips appear synchronously to *Trigger* signal: just when shaped signal reach its

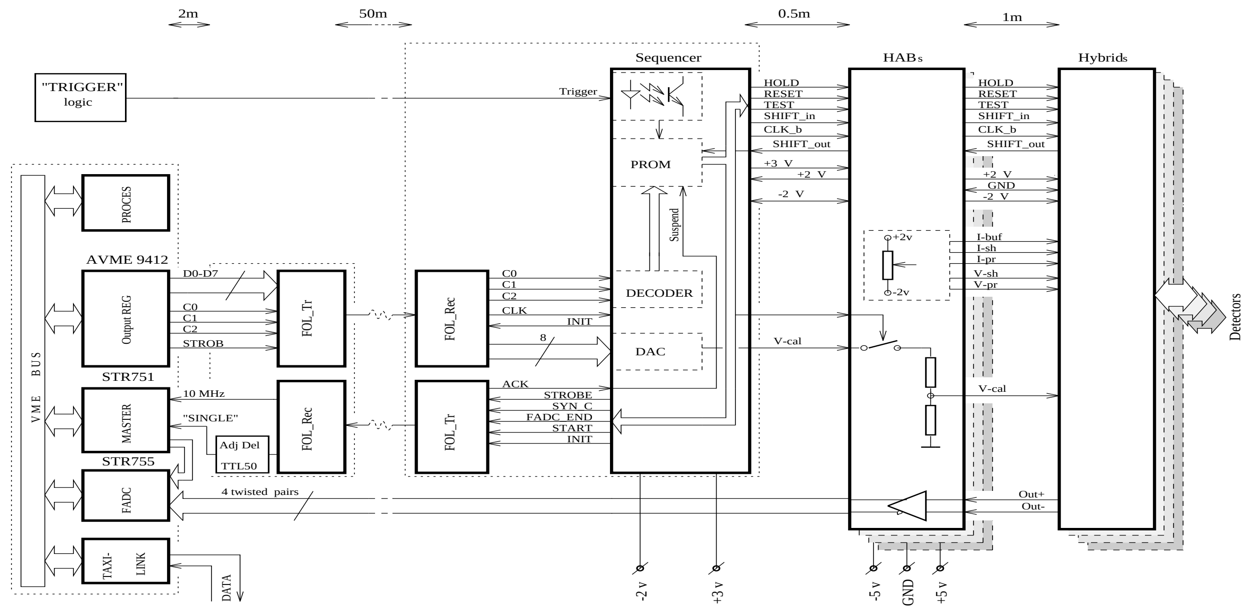

Figure 1: Block diagram of the readout system.

peak. Then read-out sequence of control signals for VA1 is started. The train of 1024 of stored analog signals appear on the output of multiplexer, and after buffer they are sent to FADC. The synchro-signals from *Sequencer* for sampling of FADC (*Single*) are sent by FOL to FADC. When the output daisy-chained signal $Shift_{-out}$ from the last VA1 chip on hybrid come to *Sequencer* the read-out will stop. The frequency of shifting of analog data is 2.5 MHz – so digitization time of our detector is 0.4 ms in *Normal* mode.

In the *Test* mode the calibration signal (with the amplitude determined by DAC on *Sequencer*) is applied to the input of each preamplifier in serial order using input multiplexer. The **control synchro-signals** in this mode **are sent by VME output register through FOL**. After each calibration synchro-signal the *Sequencer* provides the appearance of analog output signal for this channel and corresponding synchro-signal for sampling of FADC. The read-out timing in this mode is determined by VME based processor. (**Each 2 first channels of each VA1 chip require delay between CLK and Calibration signal to be** $\sim$**2** ms, for the rest of 126 channels such delay should be $> 50\ \mu s$.

Because in such approach the common capacitor is used for calibration of all 128 channels of a VA1 chip, the good relative gain information is provided.

The measured noise of VA1 channels in the "*Test*" mode is larger than in "*Normal* mode (2.5 and 0.84 ch correspondingly), and depends on the length of cable between HAB and hybrid.

1 How to handle with WA98 Si-detector ...

- NIM-FOL module with FOL should be connected to AVME-9412 module by flat cable with $pull-up$ resistor (see Fig.2). STR751 and STR755 should be connected by 20 cm long cable with "twisted" conductors. There should be *jumper* on the top of the top 34-pin flat cable

connector of NIM-FOL module. Gray 50 long cable with flat cable attached at the end, should be connected to $ANALOG$ input of STR755. LEMO connections:
$TEST-OUT_{STR751} \longleftrightarrow TEST-IN_{STR755}$
$10MHz_{NIM-FOL} \longleftrightarrow CLOCK_{STR751}$
$SINGLE_{NIM-FOL} \longleftrightarrow SINGLE_{STR751}$.

- **100 m fiber optic cable** should: $TRANSMITTER_{Sequencer} \rightarrow RECIEVER_{NIM-FOL}$
  the second fiber optic cable (now 150 m): $TRANSMITTER_{NIM-FOL} \leftarrow RECIEVER_{Sequencer}$.

- Low frequency (50-60 Hz) power supply unit (5 V for *Sequencer*, ± 5 V for HAB) should be connected to $\approx$ 220 **V power net.**

- 4 flat cables from HAB should be connected to 34-pins connectors on SPMD (by cables "out" of SPMD) as shown on Fig.4. The same for 6-pin biasing connectors which should be connected to "Trigger-boxes". (**Unfortunatelly**, each of pair of "parallel" connectors on each hybrid has one with broken wires... **The good 34-pin connectors are shown by filled circuits, the good 6-pin connectors – by filled square**).

- **16-wires flat cable** which connects all 4 "Trigger-boxes" should:
  be connected to "Plastic-box" (12*6*2 cm^3 and powered (?) at one end,
  and **should have "special" wire connected to -2 V at 34-pin connector** of SPMD (see Fig.5).

- Schematic connections of SPMD are shown on FIG.3.
  The input "TRIGGER" signal for "*Sequencer*" should be **"+TTL-50Ω"** signal with the **lenght more than 150** ns, and with *rising* **edge dalayed by 600 ns after particle**.

- Switches which control the fans of *Sequencer* and HAB should be "ON".

- The proper sequence of "power on" of SPMD is the following:
  Turn the switches "ON" in the order: left, right, middle.
  Set zero voltage on the HP-bias voltage power supply, and turn it on.

- *Sequencer* should be initialized by AVME-9412 according to the list of commands shown below (at the end).