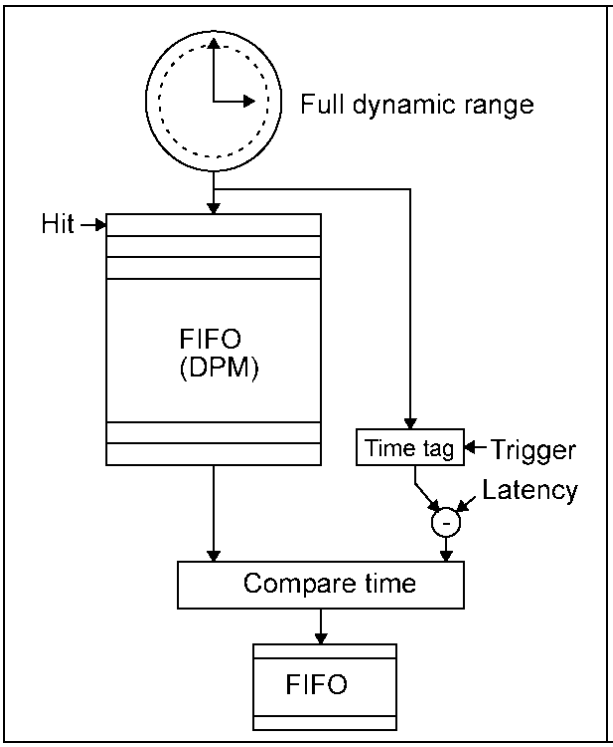
New Time Measurement System for PHOBOS

Technical specifications of the proposed system

Number of channels:	**512**
Number of channels per board	32 (in VHR mode), 64 (in HR mode)
Data transfer rate to DAQ:	6 MB/s, **(1.5 M** Hits/s or **3000** Hits/event for 500 Hz DAQ**)**
Data transfer channel	100 Mbps Ethernet or FPDP
VME access	A24D32, D32 BLT and CBLT, MCST
Clock frequency:	40 MHz
Time bin size:	25 ps (in HR mode), or 100 ps (in HR mode)
Differential non-linearity:	+1.3, -0.7 bin
Integral non-linearity:	+3.5, -5.3 bin
Time resolution:	0.5 bin RMS (50 ps) in HR mode
	2.4 bin RMS (58 ps) in VHR mode
	0.7 bin RMS (17 ps) table corrected
Variation with temperature:	Max. 100 ps change with 10 Deg. change of IC temp.
Cross talk:	**Max. 150 ps** from concurrent 31 channels to one
Dynamic range:	12+8+2 = 22 bits
Double pulse resolution:	Typical 5 ns. Guaranteed 10 ns
Max. recommended Hit rate:	8 MHz per channel
Event buffer size:	4*256
Read-out buffer size:	256
Trigger buffer size:	16
Max. recommended trigger latency:	25 μs

HPTDC

The system is based on the HPTDC – general purpose High Performance TDC, version 2.1, developed in the Microelectronics group at CERN. The data driven architecture of the TDC has proven to be extremely flexible and work well in many different kinds of experiments. The version 2.1 is the latest version of the TDC and is successfully used in NA48 and planned for CMS Muon (10000 TDCs), ALICE TOF (24000 TDCs) experiments at CERN. A trigger matching function based on time tags allows the trigger latency to be programmable over a large dynamic range and also insures the capability of supporting overlapping triggers, where individual hits may be assigned to multiple events.



Data driven TDC

- Variable latency over full dynamic range
- Triggered / non triggered mode
- Multiple overlapping triggers
- Good double pulsing resolution
- High flexibility

Fig. 1. The HPTDC. The time of the hit arrival is digitized using 320 MHz counter. The Delay Locked Loop (DLL) is used to improve the time resolution to 100 ps. By performing multiple sampling of the DLL signals, controlled from a precisely calibrated R-C delay line, the time resolution is improved further to 25 ps. The hits are stored in the L1 FIFO. The trigger stamps are registered in the 16 deep Trigger FIFO. The hit matching is performed by searching the hits in the L1 buffer within the predefined window. The matched hits are stored in the output FIFO.

For the purpose of PHOBOS the two modes are considered: VHR - very high resolution (25 ps bin) and HR - high resolution (100 ps bin). In both modes the core of the TDC is identical, the higher resolution in VHR achieved by combining four channels, each shifted by 25 ps using precise internal RC delays. The VHR mode is the normal mode for TOF operation, it matches the intrinsic resolution of the TOF (70 ps).
The description of the HPTDC can be found at
http://micdigital.web.cern.ch/micdigital/hptdc.htm.

Problem with HPTDC and a workaround

L1 buffer parity error gets detected internally in chip depending on use and logic core power supply voltage.
L1 buffer parity error gets set in JTAG status and measurement is ignored in trigger matching (not read out)
Problem occurs at increased Vdd (highly uncommon failure mechanism)
Seen for first time in latest version (Earlier version do not have this problem up to 3.0 volt)

Workaround

In our design we will be using reduced power supply voltage 2.3 V.
The group has experience of running the similar system using the same version TDC in KABES readout at NA48 at CERN. The problems were carefully studied and found a way to run TDC successfully.

Triggering

The HPTDC is designed for LHC therefore it requires the clock period equal to 25 ns which is different form the RHIC RF period of 36 ns.

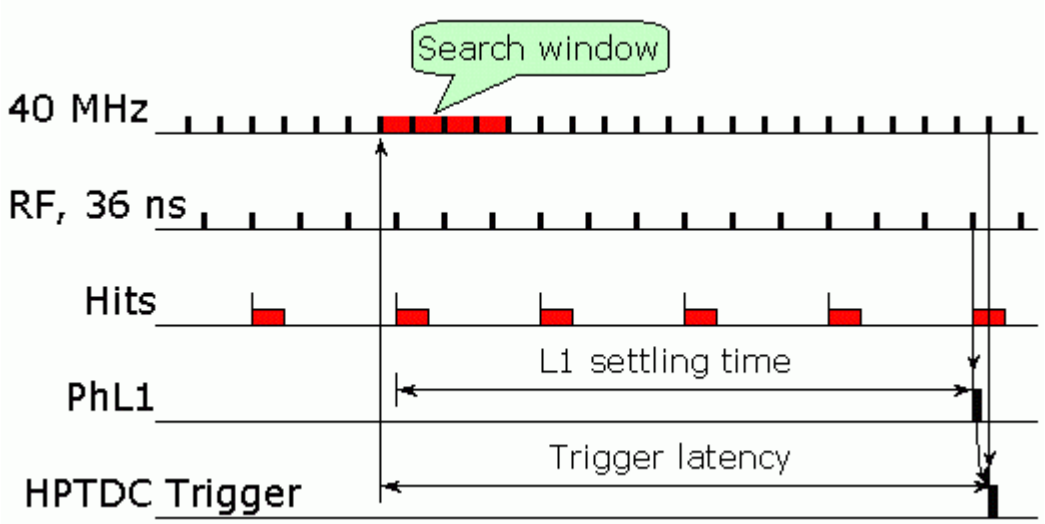


Fig.2. Triggering of the PhTimes. All HPTDCs are running from the global 40 MHz clock. But the PHOBOS L1 trigger is synchronized with the RHIC RF 28 MHz, therefore this trigger should be resynchronized with the 40 MHz clock before sending to HPTDCs.

An important point in the use of the trigger matching function of the HPTDC is that the HPTDC trigger must be given as a clock synchronous signal with a fixed latency.
The main PHOBOS trigger (PhL1) is synchronized with the bunch crossing and has fixed delay relative to it. Therefore, the PhL1 should be resynchronized with the global HPTDC clock (40 MHz) before sending to the HPTDC. The trigger latency should be set to (L1 setting time)/25 + 2 clocks.

Construction

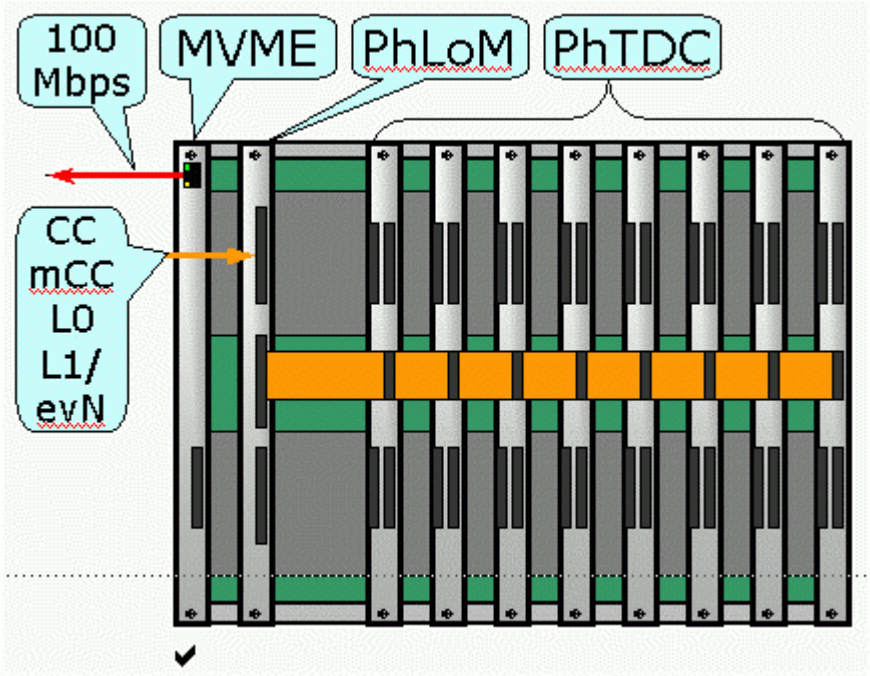


Fig 3. PhTimes VME crate consist of 16 PhTDC boards with 32 TDC channels on each, logic module PhLoM for distributing clocks and synchronization with DAQ, the general purpose VME CPU – MVME. The data from the PhTDCs are collected by MVME and sent to the DAQ over Fast Ethernet.

PhTDC: VME A24D32 slave, capable of CBLT – chained block transfer and MCST multicast commands.
PhLoM: VME A24232 slave. Accepts from DAQ crossing clock, master crossing clock, PhL1 and the event number. Generate for PhTDCs global clock 40 MHz, trigger and reset.
MVME: general purpose CPU, MVME 2600 with Ethernet connection to DAQ

The data are transferred to DAQ using RS 485 link from PhLoM or using Fast Ethernet at 6 MB/s.
At such rate the system can handle up to 3000 events per second with 100% of hit occupancy.

Cost breakdown

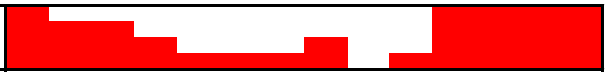
Total system cost:				$35,150
Last updated June 1, 2003				
Number of channels:		500		
TOF. 240 slats, 2 channels per slat		480		
T0		20		
Number of PhTDC boards		17		
Number of spare boards/channels		1	12	
TDC channels per ROC		32		
Resolution [ps]		25		
Combining factor		1		
Cost of all PhTDC boards	Qty	Price	Subtotal	$24,642
Total number of boards	17	$1,450		
Number of HPTDC per board	4	$46		
Design	1	$3,000	$3,000	
Components	17	$785	$13,342	
PCB Setup	1	$500	$500	
PCB per board	17	$150	$2,550	
Assembly setup	1	$1,000	$1,000	
Assembly per board	17	$250	$4,250	
PhLoM. PHOBOS Logic Module	Qty	Price	Subtotal	$10,100
Total number of boards	4	$2,525		
Design	1	$3,000	$3,000	
Components	4	$1,000	$4,000	
PCB Setup	1	$500	$500	
PCB per board	4	$150	$600	
Assembly setup	1	$1,000	$1,000	
Assembly per board	4	$250	$1,000	

Not included: living expenses for two persons from Dubna for one month.

Production schedule

Production schedule of the PhTiMeS														
Week		1	2	3	4	5	6	7	8	9	10	11	12	13	14
Design of 25 ps PhTDC	SB														
Design of of the PhLoM	SB														
Searching for components	AS														
Ordering components.	AS														
PCB Production	AS														
PCB Assembly	AS														
Debugging. SB at BNL	SB														

Money flow														
Components			$17,342										$408	
PCB Setup					$4,150									
Assembly setup								$7,250						
Crate										$0				
S-Link										$0				
Not assigned													$6,000	
Total													$35,150	

Manpower. BNL Man-weeks	100% 0%	

The system can be completed for 14 weeks from the approval. As of July 2 2003 the schematic design of the PhTDC have finished.